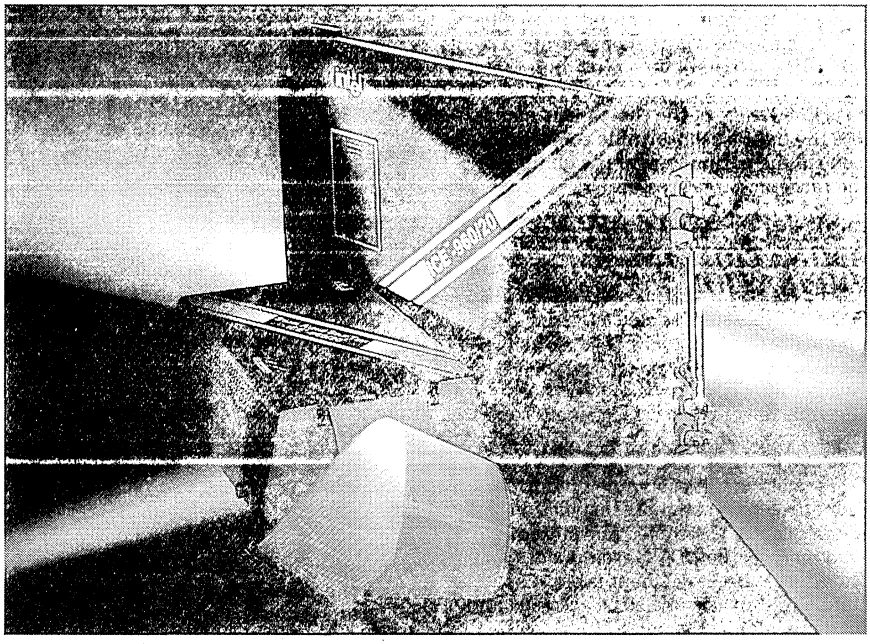
ICE™-960MC IN-CIRCUIT EMULATOR



280899-1

IN-CIRCUIT EMULATOR FOR THE 80960MC MICROPROCESSOR

The ICE™-960MC In-circuit Emulator delivers real-time hardware and software debugging capabilities for 80960MC based designs. Features include emulation of the 80960MC microprocessor, powerful breakpoint specification, fastbreaks, optional relocatable expansion memory, two types of trace capability, large trace buffering, support of virtual and physical component addressing modes, and sophisticated human interface. The ICE-960MC In-circuit Emulator gives you unmatched control over all phases of hardware/software debug, including developing, integrating and testing, which improves development productivity and speeds time to market.

FEATURES

- Real-Time Emulation of the 80960MC microprocessors up to 20 MHz (25 MHz optional)
- Full Symbolic Information Relating to Code. Data symbolics subject to some limitations in virtual addressing mode
- Optional ICE960KBREM Board Provides 2 Mbytes of ICE Memory Which Can Overlay User ROM or RAM.
- Zero wait-state operation from user memory
- Examine and modify Memory and the 80960 Registers
- Breakpoint Capabilities include: Execution Address, Instruction Type, Bus Read/Write/Access, and Data Value. Qualification of Events is Based on an Occurrence Counter and an 8 state State-Machine
- Hosted on IBM PC AT or compatible
- Dynamically monitor or update program variables or memory during emulation with Fastbreaks
- 1024 Frame Trace Buffer for execution and/or Bus Trace and time tags
- 256 Kbytes of Memory in Standalone Self-Test (SAST) Unit

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ICE™-960MC IN-CIRCUIT EMULATOR

REAL-TIME EMULATION

The ICE-960MC In-circuit Emulator provides emulation of the 80960MC at speeds up to 20 MHz (25 MHz optional), thus providing early detection of subtle timing problems. Intel's intimate knowledge of the component makes possible the tightest conceivable conformance between timing parameters of the emulator and the target microprocessor.

PROCESSOR/MEMORY EXAMINATION AND MODIFICATION

The 80960MC registers can be accessed mnemonically (e.g. g12, r5, fp3) with the ICE-960MC emulator software. Data can be displayed or modified in one of four bases (hexadecimal, decimal, octal, or binary) and by data type (byte, word, etc). Program memory contents can be disassembled and displayed as 80960 assembly instruction mnemonics. Additionally, 80960 assembly instruction mnemonics can be assembled and stored into program memory. 80960MC system data structures such as the segment table, dispatch port, and page tables can also be accessed and modified mnemonically.

PROGRAM TRACING

The ICE-960MC emulator can store 1024 frames of program execution history or 1024 frames of the 80960MC address/data bus activity in the trace buffer. Each frame of program execution contains a discontinuity address (branch, call, return, etc) and a time-tag. This information can be used to reconstruct a history of the program execution. With the execution trace option enabled, the ICE-960MC will run at less than full speed. Each trace frame of bus cycles contains one complete bus burst trace. Collection of trace information is controlled by a logic analyzer type moving trace window and by bus access type.

EVENT RECOGNITION (BREAKPOINT CONTROL) AND EMULATION CONTROL

ICE-960MC provides comprehensive event recognition capabilities including: two hardware and thirty-two software breakpoints for instruction execution breakpoints, and use of the internal debug registers to recognize execution of certain instruction types such as branch or call instructions. Bus analysis logic provides recognition of external bus addresses qualified by read, write, or access type as well as data values which may be entered as masked values. Two synchronization lines are provided for recognition of external events. ICE-960MC also provides qualification of events based on an occurrence counter or by a recognition sequence of up to 8 events. Special additions for the 80960MC include the ability to recognize process binds. Additionally, emulation can be automatically stopped when the trace buffer is full. Besides the ability to execute program code at full speed between specified points, the ICE-960MC emulator provides the capability to single-step through program code.

RELOCATABLE EXPANSION MEMORY

An optional board provides ICE-960MC with 2 Mbytes of relocatable expansion memory which allows users to develop applications either before the target system memory is working, or in place of ROM or EPROM to speed the debugging cycle. This memory can be mapped in two separate 1 Mbyte partitions on 1 Mbyte boundaries. The memory waitstate pattern is (3,1,1,1) when the user's system does not return RDY# for accesses directed to the ICE960KBREM board. For accesses where the user system does return RDY# the waitstate pattern will be the larger of (3,1,1,1) or user waitstate pattern plus (2,2,2,2). The size and shape of the board is identical to the ICE probe and is installed between the probe and the user's target system when in use. The memory configuration can be mapped via either an ICE MAP command or via switches on the ICE960KBREM board.

The ICE-960KBREM card adds some constraints when used with the ICE in a user's target system. First, users should qualify bus drivers/buffers with DEN# in order to eliminate potential bus conflict between REM960 and their target memory. Second, the 1 Mbyte partition size can not be reduced and may effect the design of the user's memory subsystem. Third, ICE960KBREM delays the ADS# and DEN# signals by 5 nsec (typical) and delays the RDY# signal by 2 nsec (typical). Fourth, it adds loading, capacitance, and power requirements as shown in tables 3 and 4.

ICE™-960MC IN-CIRCUIT EMULATOR

STANDALONE OPERATION

Product software can be developed and debugged prior to and independent of hardware availability with the Standalone Self Test unit (SAST), which contains 256 Kbytes of two wait-state program memory. The SAST also provides diagnostic testing to assure full functionality of the ICE-960MC emulator.

VERSATILE AND POWERFUL HOST SOFTWARE

ICE-960MC provides an easy-to-use human interface which utilizes color and pull-down menus to complement a powerful command set. The software includes: an on-line help facility, a dynamic command entry and syntax guide, screen oriented editor, assembler and disassembler, input/output redirection, command piping, DOS command entry, and the ability to customize the command set via debug procedures and literal definitions.

Special software commands are provided to display, interpret, and modify the 80960MC hardware data structures including the segment table, dispatch port, process control block, and the page tables and directories.

DEBUG PROCEDURES AND LITERALS

Debug procedures (PROCs) are user-defined groups of ICE-960MC emulator commands. They can be stored on disk and recalled during later debugging sessions. PROCs can be used to simplify the process of debugging by grouping repetitive emulator commands, which can then be accessed by typing the name of the PROC. Literals are user-defined abbreviations for whole or partial ICE-960MC emulator commands. Literals are a shorthand method of customizing the emulator commands to fit your needs and preferences.

ICE™-960MC IN-CIRCUIT EMULATOR

WORLDWIDE SERVICE, SUPPORT, AND TRAINING

To augment its development tools, Intel offers a full array of seminars, classes, and workshops, field application engineering expertise, hotline technical support, and on-site service.

Intel also offers a Software Support package which includes technical software information, telephone support, automatic distribution of software and documentation updates, access to the "ToolTalk" electronic bulletin board, "*iComments*" publication, remote diagnostic software, and a development tools troubleshooting guide.

Intel's Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

SPECIFICATIONS

HOST REQUIREMENTS

IBM PC AT (minimum requirements) with 640 KB of conventional memory

- 1 MB of RAM (Lotus, Intel, Microsoft expanded memory specification)
- 20 MB Fixed Disk
- At least one 5-¼" Floppy Disk drive
- A serial interface
- DOS Operating system (version 3.2 or later excluding 4.x)

REQUIRED SYSTEM RESOURCES

The ICE-960MC emulator requires the following: a) exclusive use of the 80960MC's on-chip debug registers and b) a minimum of 256 bytes of target system RAM used to flush the 80960 local registers.

Mechanical Specifications

TABLE 1. ICE-960MC Emulator Physical Characteristics

	Width		Height		Length		Weight	
Unit	**Inches**	**cm**	**Inches**	**cm**	**Inches**	**cm**	**lbs**	**kg**
Control unit	10.5	26.7	1.5	3.8	16.0	40.6	6.0	2.72
Processor module*	3.8	9.6	1.5	3.8	5.0	12.7		
SAST	6.0	15.2	2.0	5.1	8.0	20.3	3.5	1.59
OIB	3.8	9.6	.9	2.3	5.1	13.0		
Power supply	2.8	7.1	4.2	10.7	11.0	27.9	4.7	2.14
User cable					22.0	55.9		
Serial cable					12.0 ft	3.66m		

*measurement includes target adaptor

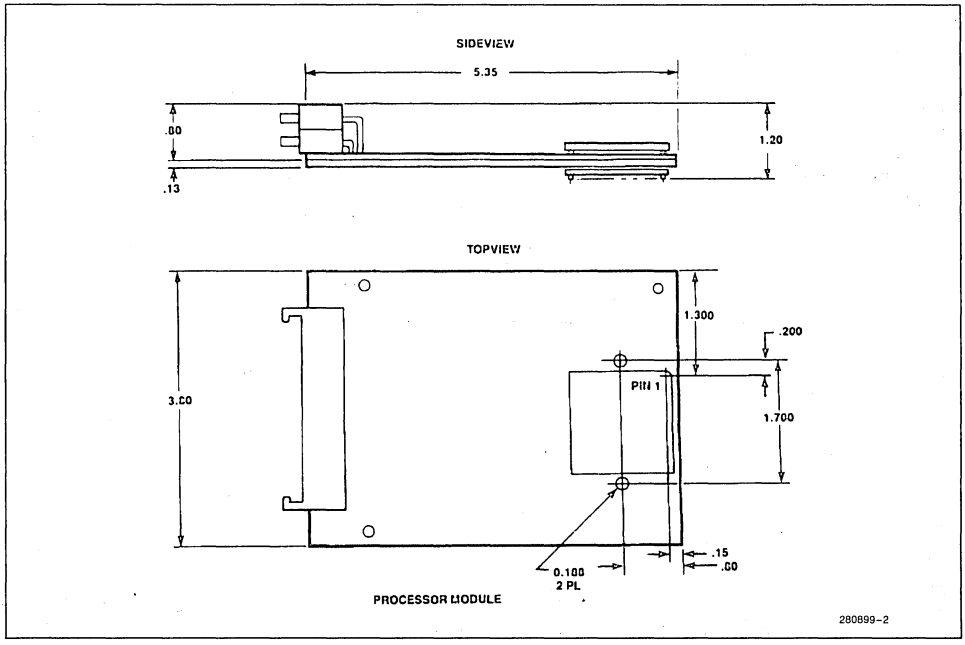

Figure 1: Processor Module

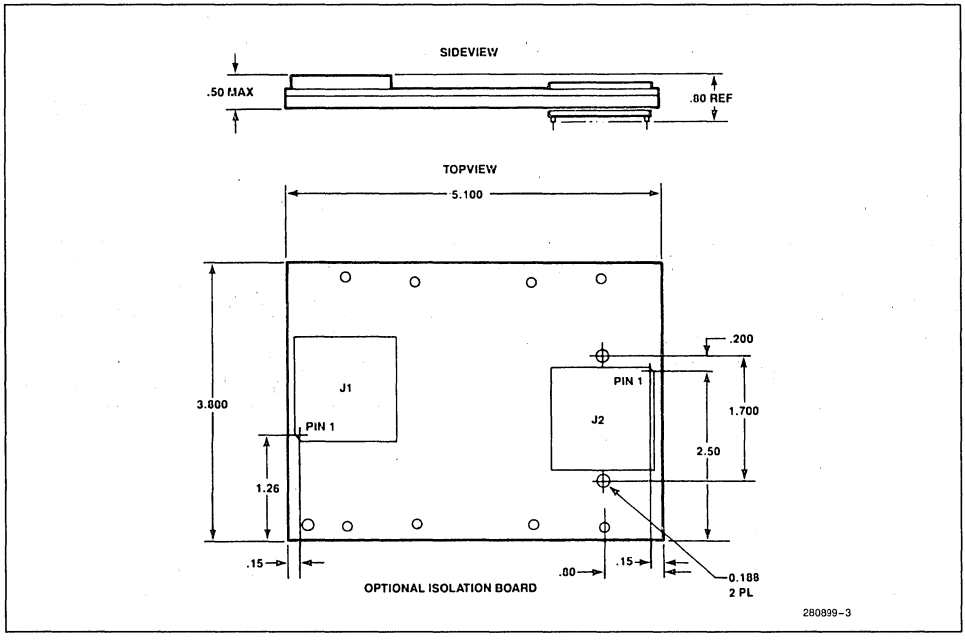

Figure 2: Optional Isolation

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

SYNC Line Specification

The SYNCIN line must be valid for at least one instruction cycle because it is only sampled on instruction boundaries. The SYNCIN line is a standard TTL input. The SYNCOUT line is driven by a TTL open collector with a 4.75K-ohm pull-up resistor.

AC/DC Specifications

The Optional Isolation Board (OIB) isolates the ICE-960MC probe from an untested user target system. When the OIB is in use, the ICE-960MC AC and DC specifications differ from the 80960MC microprocessor as shown below. When the OIB is not installed, the ICE-960MC specifications are identical to those of the 80960MC component.

TABLE 2. AC Specifications With The OIB Installed

Symbol*	Parameter	Minimum	Maximum
t2	clock low time	2+1nS	
t3	clock high time	3+1ns	
t6	output valid delay		
	A/D 0:31	6+8ns	t6+16Ns
	DT/R#, DEN#, BE0-3#, ADS#, W/R#	6+7nS	t6+14ns
	HLDA, CACHE, LOCK#, INTA#	6+6ns	t6+8nS
	ALE#	6+10nS	t6+20nS
t7	ALE# width	7−6.5nS	
t8	ALE# disable delay	8+nS	t8+14nS
t9	output float delay		
	A/D 0:31	t9+5nS	t9+22nS
	DT/R#, DEN#, BE0-3#, ADS#, W/R#	t9+7nS	t9+15ns
	HLDA, CACHE, LOCK#, INTA#	t9+6nS	t9+8nS
t10	input setup 1		
	A/D 0:31	t10+2nS	
	BADAC#, INT0-3# deassertion	t10+14nS	
t11	input hold		
	A/D 0:31, HOLD	t11+6nS	
	BADAC#, INT0-3#,		
	READY#	t11+7nS	
t16	reset setup time	16+6	

*symbol refers to 80960MC specification

TABLE 3. ICE-960MC Emulator DC Specifications

Symbol*	Parameter	Maximum
PM-Icc	Supply current with 80960KB-20	1400mA
OIB-Icc	Supply current	PM-Icc + 1100mA
REM-Icc	Supply current	PM-Icc + 1300mA (1700 Total Typical)

SPECIFICATIONS

TABLE 4. Additional DC Loading

Signal	(without OIB installed) Iih Maximum	(without OIB installed) Iil Maximum	(with OIB installed) Iih Maximum	(with OIB installed) Iil Maximum	(with REM installed) Iih Maximum	(with REM installed) Iil Maximum
AD (0:31)	100 uA	0.6 mA	20 uA	−1 mA	120 uA	0.7 mA
ADS#	140 uA	1.6 mA	20 uA	−1 mA	Driven by 74AS760	
DEN#	40 uA	1.0 mA	20 uA	−1 mA	w/ 4.7k pull-up	
W/R#	140 uA	1.6 mA	20 uA	−1 mA	150 uA	1.7 mA
CLK2	80 uA	2.2 mA	50 uA	−2 mA	130 uA	2.9 mA
RESET			50 uA	−2 mA	250 uA	0.3 mA
BE (0:3)#			20 uA	−1 mA	10 uA	0.1 mA
READY#			20 uA	−1 mA	750 uA	0.8 mA
ALE#			20 uA	−1 mA	20 uA	0.5 mA
DT/R#			20 uA	−1 mA		
INTO#, INT3#			20 uA	−1 mA		
INT1, INT2			20 uA	−1 mA		
BADAC#			20 uA	−1 mA		
LOCK#			20 uA	−1 mA		
HOLD			20 uA	−1 mA		
FAILURE#			20 uA	−1 mA		

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SPECIFICATIONS

POWER SUPPLY

100–120V or 220–240V (Selectable)
50–60 Hz
2 amps (AC Max) @ 120V
1 amp (AC Max) @ 240V

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature	10°C to 40°C (50°F to 104°F)
Operating Humidity	Maximum 85% Relative Humidity, non-condensing

ORDERING INFORMATION

Order Code	Description
ICE960MC	The complete 20 MHz ICE-960MC emulator system including control unit, processor module, power supply, SAST, OIB, SAB, serial communications cable (SCOM4), IEDIT, V1.0 software. (Requires software license, Class I)
ICE960MC25P	25 MHz ICE960MC as described above
I960MCUPG	Conversion kit to convert ICE-960KB to ICE-960MC. Consists of new host and probe software, probe firmware, and manual. Requires ICE-960KB V2.0 hardware.
ICE960KBREM	Optional 2 Mbyte Relocatable Expansion Memory Board.